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Designing of Combinational Circuits from Reversible Decoder Circuit

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Abstract- Reversible logic is that the rising field for analysis in present era. The aim of this paper is to understand differing kinds of combinational circuits like full-adder, full-subtractor, multiplexer device and comparator victimization reversible decoder circuit with minimum quantum cost. Reversible decoder is meant victimization Fredkin gates with minimum Quantum value. There square measure several reversible logic gates like Fredkin Gate, Richard Phillips Feynman Gate, Double Richard Phillips Feynman Gate, Peres Gate, Seynman Gate and plenty of additional. Reversible logic is outlined because the logic in which the amount output lines square measure up to the amount of input lines i.e., the n-input and k-output mathematician perform F(X1, X2, X3,…, Xn) (referred to as (n, k) function) is alleged to be reversible if and provided that (i) n is up to k and (ii) every input pattern is mapped unambiguously to output pattern. The gate should run forward and backward that's the inputs can even be retrieved from outputs. once the device obeys these two conditions then the second law of thermo-dynamics guarantees that it dissipates no heat. Fan-out and Feed-back don't seem to be allowed in Logical changeability. Reversible Logic owns its applications in varied fields that embrace Quantum Computing, Optical Computing, engineering, Computer Graphics, low power VLSI Etc., Reversible logic is gaining its own importance in recent years mostly because of its property of low power consumption. The comparative study in terms of garbage outputs, Quantum value, numbers of gates also are presented. The Circuit has been enforced and simulated victimization Xilinx software package.

Index Terms- Quantum cost, Reversible gates, Garbage outputs, number of gates, Delay.

1. INTRODUCTION

In present VLSI Technology, Power Consumption has become an awfully necessary issue for thought. By using Reversible Decoder for planning combinatory circuits power consumption is reduced to associate degree optimum once compared to traditional decoder primarily based combinatory circuits. Reversible Logic finds its own application in Quantum computing, nano-technology, optical computing, computer graphics and low Power VLSI. Ralf Launder told that cooling in circuits isn't thanks to the process concerned within the operation; however it's attributable to the bits that were erased throughout the method. He introduced that losing of one bit within the circuit causes the tiniest[1] amount of warmth within the computation that is adequate KTln2 joules wherever K is physicist constant and T is Temperature. The amount of warmth dissipated in easy circuits is extremely small however it becomes massive within the complicated circuits that imply propagation delay conjointly. Later in 1973 C. H. Bennett delineated that the ability dissipation attributable to the bit loss can be overcome if every and each computation in circuit was disbursed in reversible manner. Quantum networks square measure designed of quantum logic gates[2]. As every gate perform a unitary operation, KTln2 Joules energy dissipation wouldn't occur if the computation is disbursed in reversible manner. Thus computation worn out reversible manner doesn't need erasing of bits. The quantity of warmth dissipated within the system holds an instantaneous relationship to the quantity of bits erased or lost throughout the computation[3].

2. LITERATURE SURVEY

In 1961,R.LANDAUER represented that the logical reversibility is related to physical reversibility and needs a stripped-down heat generation per machine cycle[1]. For irreversible logic computations ever little bit of data lost generates kTlog2 joules of warmth energy, wherever k is Boltzmann's constant and T absolutely the temperature at that computation is performed. In typical system the voluminous gates accustomed perform logical operations. Author verified that cooling avertable if system created reversible.

In 1973, C.H.BENNETT delineate that there will be zero power dissipation is feasible if computation is applied in Reversible logic, because the energy dissicipated[2] in the system is directly equal to the amount of bits erased throughout computation. The look that doesn't end in information loss is irreversible. a group of reversible gates are required to style reversible circuit. Reversible gate will generate distinctive output vector from every input vector and the other way around.

In 2008,Majid Mohammed et.al said that quantum gates were used for the implementation of binary reversible logic gates[3]. Quantum gates V and V+ to be pictured in fact table forms. Author proposed the area unit optimization in the reversible circuit and he had compared existing work. A replacement activit model to represent the V and V+ quantum gates supported their properties. This model accustomed simulate the quantum realization of reversible circuits.

In 2010,D.Michael Miller and Zahra Sasanian given the reducing the quantity of quantum gate price of reversible circuits[4]. To scale back the quantum price improves the potency of the circuit. To see a quantum circuit is to 1st synthesis circuits composed of binary reversible gates then map that circuit to identical quantum gate realization CMOS, Quantum laptop, and engineering science, Optical computing and self-repair.

In 2011,Md.Mazder Rahman et.al presented that library of quantum gates that consist of all doable two-Qubit quantum gates that don't turn out in twin states[5]. These gates area unit won't to scale back the quantum value of reversible circuits.
They planned a two-qubit quantum gate library that plays a major role in reducing the quantum value of reversible gates.

In 2012, B.Raghu Kanth et.al described that execution of reversible logic has advantage of less garbage outputs,constant inputs and low gate count. Addition, Subtractions operations area [6]unit complete exploitation reversible weight unit gate and it compare with standard gates. The planned reversible adder/substractor circuit will be applied to style of complicated systems in engineering science.

In 2012, Mr.Devendra Goyal bestowed VHDL CODE of all reversible gate, which give United States to style VHDL CODE [7] of any complicated sequent circuit. Here author are tried to create the VHDL code the maximum amount asdoable. Author will simulate and synthesis it exploitation it exploitation Xilinx computer codes.

In 2013, MarekSzyprowski bestowed a tool for minimizing the quantum value in 4-bit reversible circuits. Here Author shown that for benchmarks and for styles taken from recent publications it's do able to get saving in [8] quantum value examination with existing circuits.

In 2013, Raghava Garipelly as long as the essential reversible logic gates, that in coming with of additional complicated system[9] having reversible circuits as a primitive part and this could execute additional difficult operations exploitation quantum computers. Author introduced some new Gates that area unit BSCL, SBV, NCG, and PTR etc.

In 2014, AshimaMalhotra et.al delineated that reversible changed Fredkin gate wont to style the multiplexers with low quantum value and compare it with existing work[10]. They additionally compare the quantum value of multiplexer style exploitation Fredkin gate with changed Fredkin gate[12] wont to style he multiplexers.

In 2016 a novel design , the thought of reversible logic is being applied to a novel design of two to four decoder exploitation reversible logic[13] . The decoder involves [15]the employment of TR gate, CNOT gate, PERES gate that is largely a reversible gate. The circuit has been enforced in Xilinx eight.2. The machine used is Xilinx machine. The results are shown and verified with the irreversible 2 to 4 decoder.

3. CONCEPT

The Reversible Logic involves the utilization of Reversible Gates consists of a similar variety of inputs and outputs i.e., there ought to be one to 1 mapping between input vectors and output vectors. And that they will be created to run backward direction conjointly. Sure limitations are to be thought-about once designing circuits supported reversible logic (i) diffuse isn't permitted in reversible logic[4] and (ii) Feedback is additionally not permitted in reversible logic. In Reversible logic exploitation outputs we are able to acquire full data of inputs. Reversible logic conserves info. Some price metrics like Garbage outputs, variety of gates, Quantum price, and constant inputs are wont to estimate the performance of reversible circuits. Garbage outputs are the additional outputs that facilitate to make inputs and outputs equal so as to keep up reversibility.

They're unbroken alone while not acting any operations. Variety of gates count isn't a decent metric since more variety of gates will be taken along to make a replacement gate[5]. Quantum price is that the variety of elementary or primitive gates required implementing the gate. It's nothing but the quantity of reversible gates (1×1 or 2×2) needed to construct the circuit. Delay is one among the vital price metrics. A Reversible circuit style will be shapely as a sequence of separate time slices and depth is summation of total time slices[6]. In Digital physical science the binary decoder is a combinable logic circuit that converts the binary number value to the associated output pattern. Numerous proposals are given to style of combinable and sequent circuits in under going analysis. In this paper, the planning of various combinable circuits like binary comparator, Full adder, and Full subtractor Multiplexer circuits exploitation [7]Reversible Decoder is planned with optimum Quantum price.

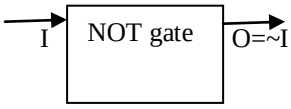
4. BASIC REVERSIBLE GATES

The basic Reversible Logic Gates gift within the literature is briefed below. The gates that area unit appropriate for the look with optimum quantum price are often elite.

4.1. *NOT gate*: The NOT GATE is that the easy Reversible computer circuit. Its 1×1 Reversible computer circuit with the quantum price zero. The Not gate merely shifts the complementary of the input to

output as shown within the figure1. it's the essential primitive gate which can involve in construction of reversible computer circuit, therefore owing its own importance in deciding the quantum price of designed Reversible computer circuit.

Table 1.Truth Table

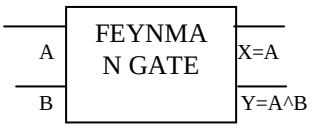


I	O
1	0
0	1

Fig.1. NOT Gate

4.2. Feynman Gate (FG): Feynman gate could be a 2×2 reversible gate as shown in below figure2. The Feynman gate is additionally referred to as as CNOT gate i.e., controlled NOT gate. The Feynman gate is employed to duplicate of the specified outputs since Fan-out isn't allowed in reversible logic gates. The Quantum price of FG is one. This is often conjointly the primitive gate owing its importance in deciding quantum price metric.

Table 2.Truth Table



A	B	X	Y
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fig.2.Feynman Gate

4.3. Double Feynman Gate (DFG): Double Feynman Gate could be a 3×3 reversible gate. The outputs area unit defined as shown within the below figure3. The quantum price of DFG is 2. This gate also can be used for duplicating outputs.

Table 3.Truth Table

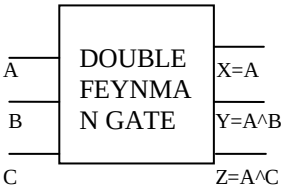


Fig.3.Double Feynman Gate

A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

4.4. TOFFOLI Gate (TG): Toffoli Gate is 3×3 reversible gate. The outputs area unit defined as shown within the below figure4. The Quantum price of TG is 4.

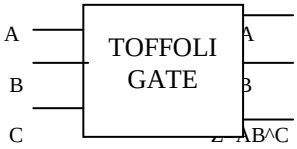


Fig.4. Toffoli Gate

Table 4.Truth Table

A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

4.5. FREDKIN Gate (FDG): Fredkin Gate could be a 3×3 reversible gate. The outputs area unit outlined as shown within the below figure4. The Quantum price of FDG is five. This paper mainly surrounds around Fredkin gate.

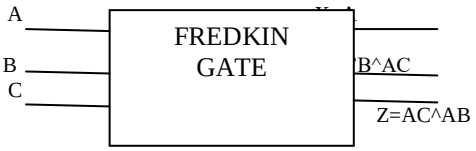


Fig.5.Fredkin Gate

Table5. Truth Table

A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

4.6. PERES Gate (PG): Peres Gate could be a could be a 3×3 reversible gate. The outputs area unit outlined as shown within the below figure6. The Quantum price of PG is four.

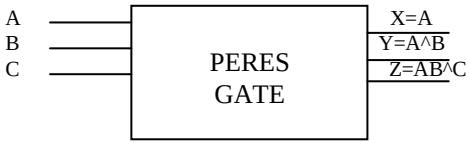


Fig.6. Peres Gate

Table 6.Truth Table

A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

4.7. TR Gate: TR Gate could be a 3×3 reversible gate. The outputs area unit outlined as shown within the below figure7. The quantum price of TRG gate is given by four.

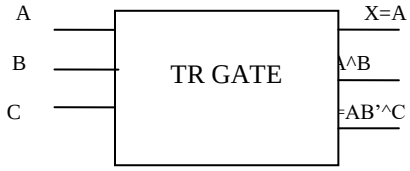


Fig.7. TR Gate

Table 7.Truth Table

A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

5.BASIC GATES USING REVERSIBLE GATES

Considering our circuit needs we want to style AND gate and logic gate mistreatment reversible gates. Here we tend to used fredkin gate to style AND and OR gates as shown in figure8. Importance is given to fredkin gate as a result of it provides optimistic performance at less Quantum price for planning AND and OR gates.

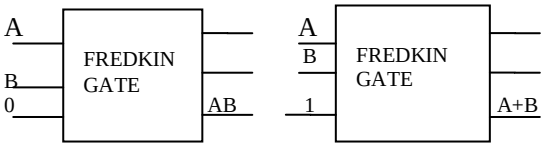


Fig.8.AND Gate using fredkin and OR Gate using fredkin

6. EXISTING METHOD

6.1. 2 to 4 Reversible Decoder

A decoder is a combinational circuit used in many devices for processing. It has multiple inputs as well as multiple outputs. Generally decoder is available as 2 to 4 decoder, 3 to 8 decoder, 4 to 16 decoder, 4 to 10 decoder. In the existing method first designed a 2to 4 decoder by using reversible gates.[8] The concept of reversible gate is input and output pins are equal. They can know the input from the output .so that when it comes to complex circuit it is easy to check whether the input of the particular gate same from the output of the before gate[9].

Here in the existing 2 to 4 decoder they have used,3 CNOT gate(Feynman gate),TR gate, one PERES gate one NOT gate, and The figure below shows the 2 to 4 reversible decoder.

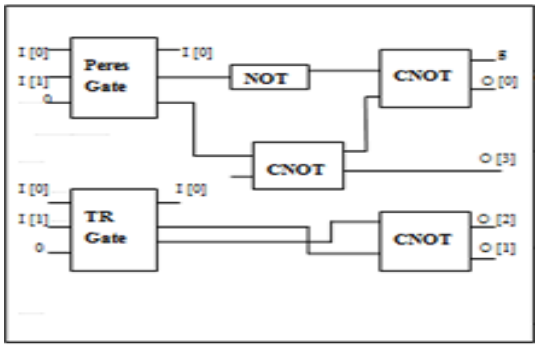


Fig 9. 2 to 4 Reversible Decoder

From the above figure two inputs I(0),Ii(1)are given to PERES gate and TR gate .The operation of the PERES gate and TR gate are explained above with their truth tables.

6.2. 3 to 8 Reversible Decoder:

The 3 to 8 reversible decoder has been designed using the 2 to 4 reversible decoder and additionally four fredkin gates. It has three input lines and eight output lines. The figure below shows the 3 to 8 reversible decoder.

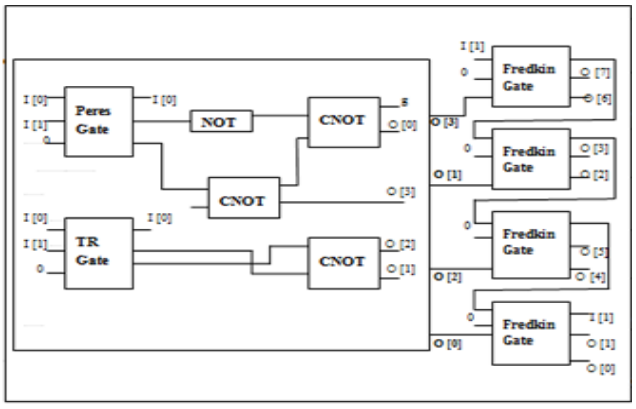


Fig.10. 3 To 8 Reversible Decoder

A 3:8 decoder has the outputsx0y0z0; x0y0z; xy0z0; xy0z; x0yz0; x0yz; xyz0; xyz.So every output of the 2:4 decoder must be increased doubly, once with z0 and so with z[10].To attain this exploitation Peres or TR gate, there'll be want of one gate for every multiplication, resulting in eight gates with a quantum price of thirty two and sixteen garbage outputs (2 for every gate).A better model are to use Fredkin gate for higher dimension. Every Fredkin gate is capable of playing 2 multiplication reducing the amount of gates to four and garbage outputs to one. The design is shown in Fig. above By using the existing method here I am designing a 4:16 decoder, eight further Fredkin gates,3 :8 decoder is required[11]. Therefore total range of Fredkin gates is twelve. Hence the quantum price is sixty and also the 2:4 decoder block prices eleven. So the ultimate quantum price of 4:16 decoder are seventy one[12].

7.PROPOSED METHOD

Different Reversible Decoder circuits like 2×4, 3×8, 4×16 are designed victimization Fredkin Gates (mainly), Feynman gates and Peres gate. Some combinatory circuits like comparator adder, subtractor, multiplexers etc., are designed victimization these decoders. The thought of duplicating one output to needed range of outputs victimization Feynman gate is introduced wherever Fan-out was not allowed in reversible computation.

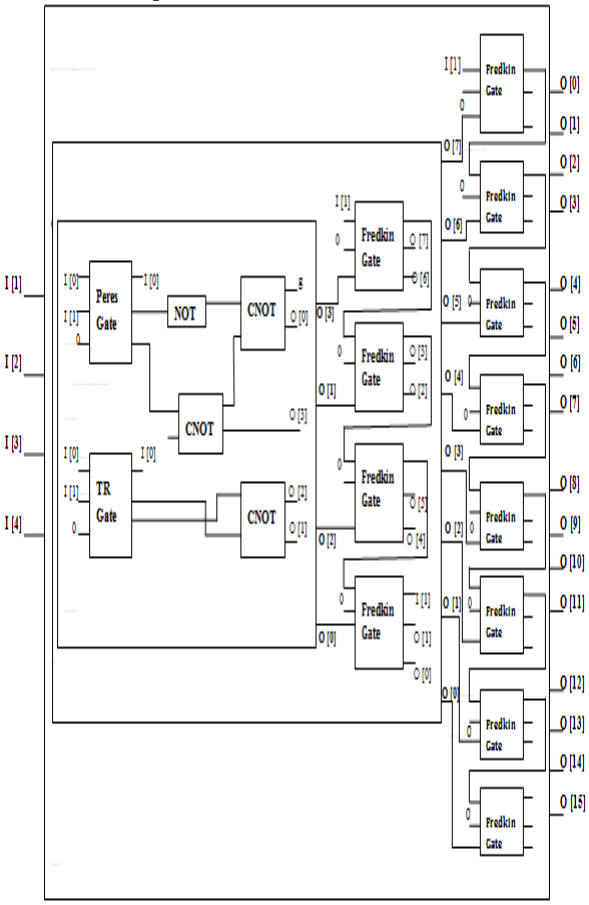


Fig .11.Block Diagram of Proposed Decoder

8.SIMULATION RESULTS OF PROPOSED CIRCUITS

8.1. 4×16 decoder

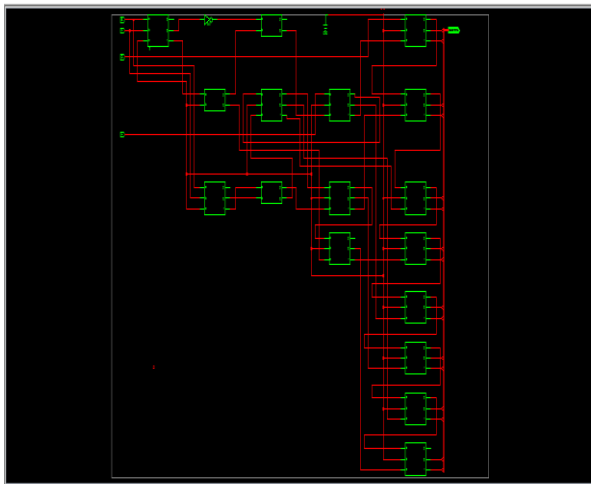


Fig.12. RTL Schematic of 4×16 reversible decoder

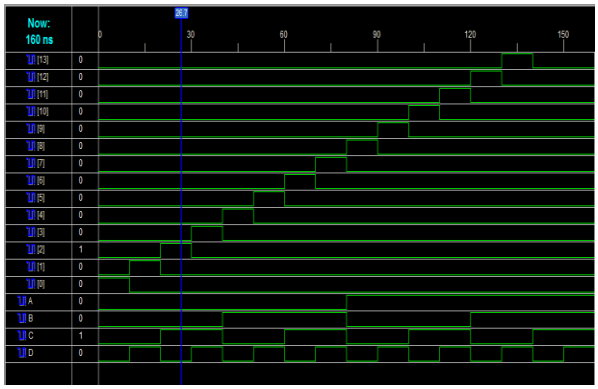


Fig.13. simulated output for 4 ×16 decoder

8.2. Binary comparator

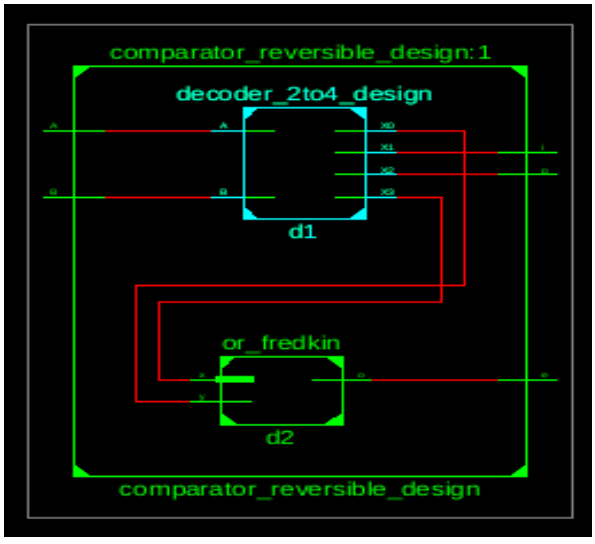


Fig.14. RTL Schematic of Binary Comparator

It is clear from the on top of simulated output in figure14 resembling step case that totally different binary number price is converted to associate pattern of outputs. The output lines g, l, e represents larger, Lesser, Equal respectively. The a, b lines represents the inputs. If a 'l' output becomes high. If a>b then 'g' output becomes high. If a=b then 'e' output becomes high.

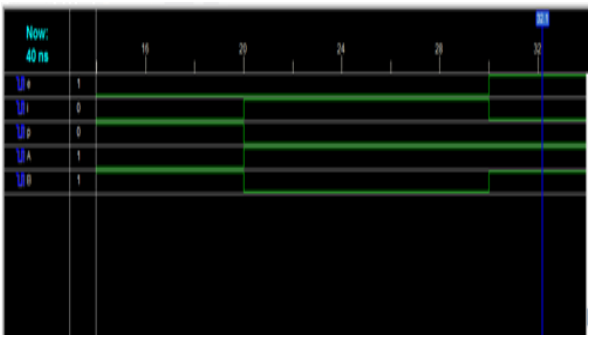


Fig.15. Simulated output for Binary Comparator

8.3. Full adder/ subtractor

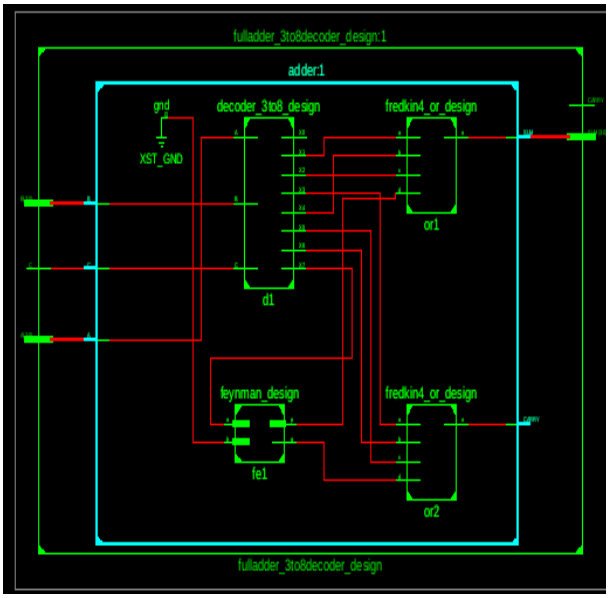


Fig.16. RTL Schematic of full adder

The idea of duplicating one output to 2 outputs victimization Feynman gate is introduced. The second input of nuclear physicist gate was created to zero that drives 2 splitted equivalent outputs.

For planning a full adder a three to eight decoder and 2 four input OR gates ar needed. The min terms for add and CARRY are derived from output pattern of decoder. Similarly the full subtractor was additionally designed.

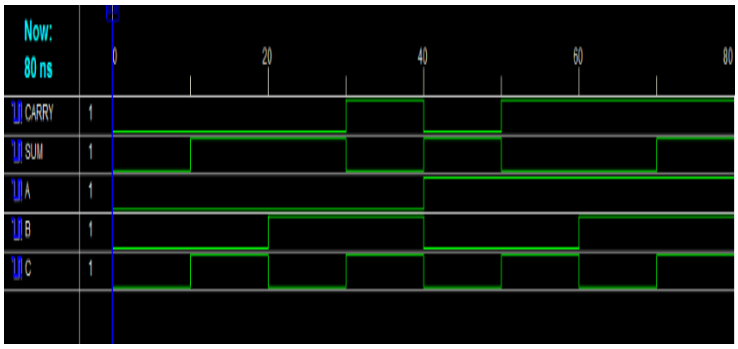


Fig.17(1). Simulated output for Full adder

Equation for carry CARRY=∑ (3, 5, 6, 7)
Equation for sum SUM=∑ (1, 2, 4, 7)
Equation for difference DIFF=∑ (1, 2, 4, 7)
Equation for borrow BROW=∑ (1, 2, 3, 7)

In the higher than min term expressions we will observe that the same min term output of decoder drives add and carry outputs of full adder (i.e., out[7] of decoder output pattern).Since Fan-out isn't allowed in reversible logic, the nuclear physicist gate is used to duplicate outputs. Equally for full subtractor outputs of decoder (i.e., out[1], out[2] and out[7]) are duplicated By using this full adder a four bit full adder/subtractor is intended. The simulated output is shown in figure17. to style 4-bit full adder/ subtractor circuit four full adders ar needed. The Cin input drives the primary full adder. If Cin is given with low input 4-bit addition is performed and if Cin is given with high input the 4-bit subtraction within the style of 1's complement addition is performed.

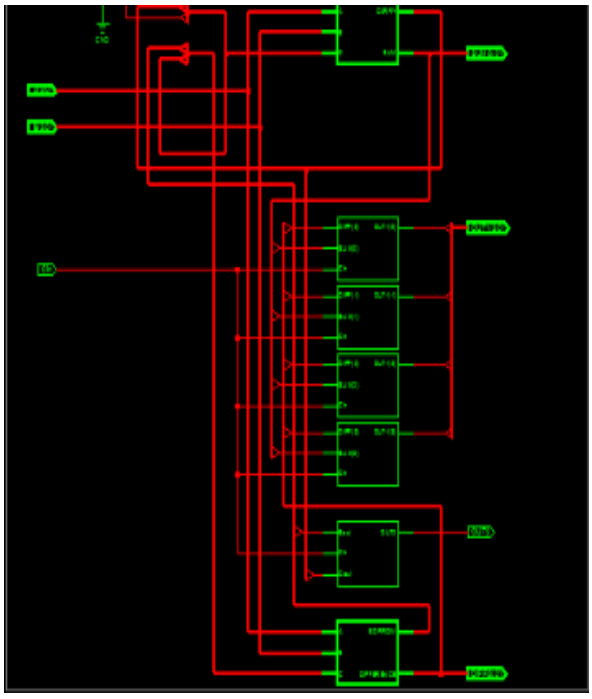


Fig.16(1).RTL Schematic of 4-bit full subtractor/adder

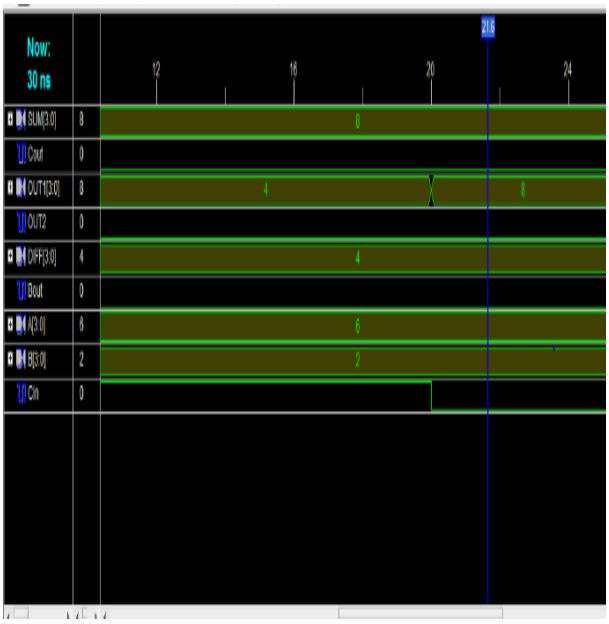


Fig.17(1). Simulated output for 4 bit Full subtractor/adder

8.4. Multiplexer

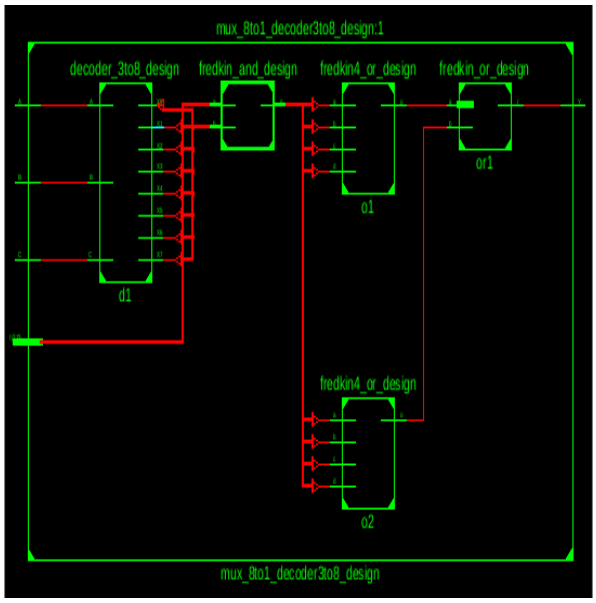


Fig.18. RTL Schematic of 8×1 multiplexer

To design multiplexer victimization reversible decoder, reversible a pair of input AND gates, a pair of input OR gates are needed. The 2 input AND gate and logic gate are designed victimization Fredkin gate. By victimization these designed gates we will improve those gates to the desired variety of input gate. Every output line from decoder is driven to a pair of input AND gate in conjunction with multiplexer input.

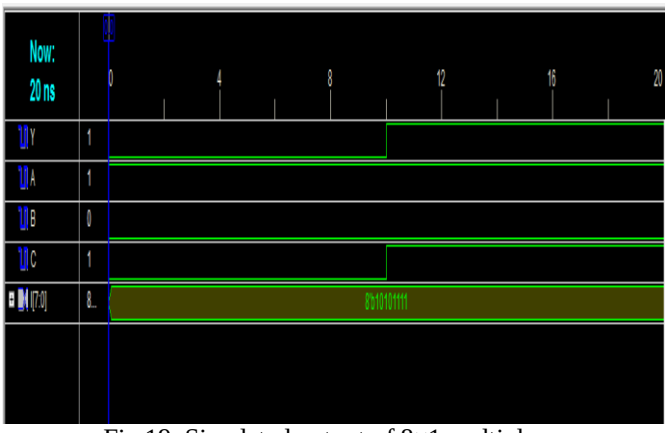


Fig.19. Simulated output of 8×1 multiplexer

The outputs of all AND gates are created to drive there to explicit input logic gate. The input binary whole number values act because the choice lines. Equally by victimization 4×16 decoder a 16×1 electronic device is meant. The RTL Schematic and the simulated outputs of 16×1 electronic device are shown in figure20.

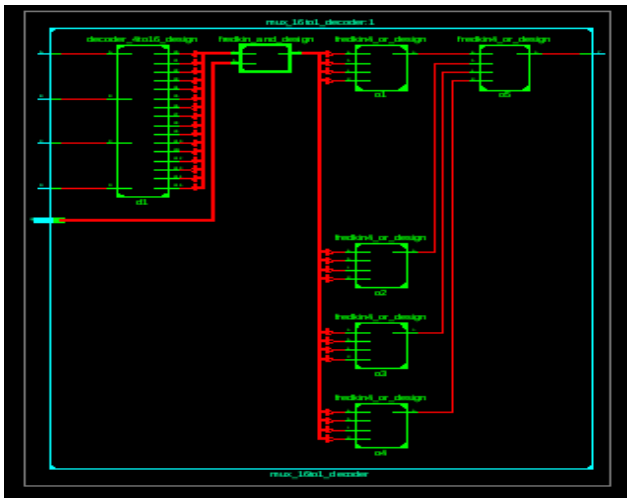


Fig.20. RTL Schematic of 16×1 multiplexer

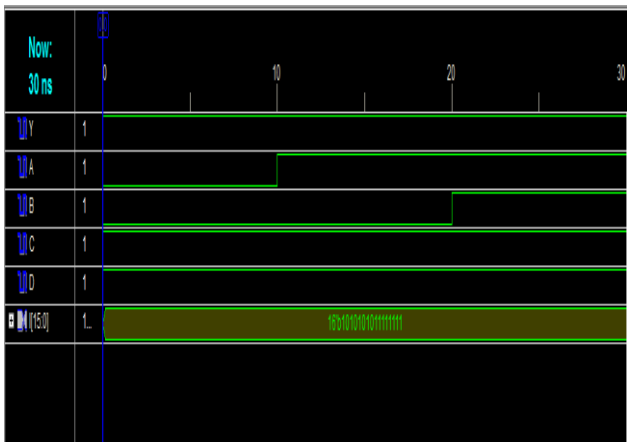


Fig.21. Simulated result for 16×1 multiplexer

9. COMPARATIVE STUDY

The combination circuits designed using reversible gates are compared with conversional combinational circuits analysed in terms of delay and number of LUTS .By using reversible circuit area is reduced.

Table 8. Comparative Study

CIRCUIT NAME	EXISTING METHOD			PROPOSED METHOD		
	Delay (ns)	Number of LUTS	Number of IOBS	Delay (ns)	Number of LUTS	Number of IOBS
4 to 16 decoder	5.924 ns	18	21	5.827ns	16	20
Binary comparator	6.657 ns	5	11	5.330ns	2	5
Full adder	6.567ns	8	19	6.49ns	6	14
8x1 multiplexer	6.842ns	16	75	5.696ns	2	12
16x1 multiplexer	6.793ns	20	80	6.652ns	5	21

10.CONCLUSION

In this paper, completely different combinative circuits like full adder, full subtractor, electronic device, comparator circuits constructed exploitation reversible decoder square measure designed. These circuits are designed for minimum quantum value and minimum garbage outputs, delay and less number of reversible gates. The strategy projected for designing the decoder circuit may be generalized. As an example, a 3×8 decoder may be designed employing a 2×4 decoder followed by four fredkin gates, equally a 4×16 decoder may be designed using 3×8 decoder followed by eight fredkin gates .The conception of duplicating the one output to needed range of outputs is utilized to beat the fan-out limitation in reversible logic circuits. This technique of coming up with combinative circuits helps to implement several digital circuits with higher performance for minimum quantum value.

REFERENCES:

[1] R. Landauer, “Irreversibility and Heat Generation in the Computational Process”, IBM Journal of Research and Development, 5, pp. 183- 191, 1961.

[2] C.H. Bennett, “Logical Reversibility of Computation”, IBM J.Research and Development, pp. 525-532, November 1973.

[3] 8]Y. Syamala, and A. V. N. Tilak, “Reversible Arithmetic Logic Unit”, Electronics Computer Technology (ICECT), 2011 3rd International, vol. 5, pp.207-211,07 july 2011.

[4] Thapliyal H, Ranganathan N.,” Design of Reversible Latches Optimized for Quantum Cost, Delay and Garbage Outputs” Centre for VLSI and Embedded

[5] William C. Athas, Lars “J” ,Svensson, Jeffrey G. koller, Nestoras Tzartzanis, and Eric Ying – Chin Chou, ”Low-power Digital Systems based on Adiabatic-Switching principle”, IEEE Transactions on VLSI systems, Vol. 2, No. 4, December 1994.

[6] J.M. Rabaey and M. Pedram, “Low Power Design Methodologies,” Kluwer Academic Publisher, 1997.

[7] T. Toffoli., “Reversible Computing”, Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science 1980.

[8] E. Fredkin and T. Toffoli, “Conservative logic,” Int’l J.Theoretical Physics, Vol. 21, pp.219–253, 1982.

[9] C H Bennett, "Notes on the History of Reversible Computation", IBM Journal of Research and Development,vol. 32, pp. 16-23, 1998.

[10] R. Feynman,”quantum mechanical computers:, Optic News, vol. 11,pp 11-20, 1985.

11] V.Rajmohan, V.Ranganathan,”Design of counter using reversible logic” 978-1-4244-8679-3/11/$26.00 ©2011 IEEE.

[12] Vivek V. Shende, Aditya K. Prasad, Igor L. Markov, and John P. Hayes,” Synthesis of Reversible Logic Circuits”, IEEE Transaction on computer-aided design of integrated circuits and systems, vol. 22, No. 6, June 2003.

[13] A. Peres, “Reversible logic and quantum computers”, phys.rev.A,Gen.Phys., vol. 32, no. 6, pp. 32663276, Dec. 1985.

[14] H.G Rangaraju, U. Venugopal, K.N. Muralidhara, K. B. Raja,”Low power reversible parallel binary adder/subtractor” arXiv.org/1009.6218,2010.

[15] Payal Garg, Sandeep Saini,"A novel design of compact reversible SG gate and its applications”,2014 14th International Symposium on Communications and Information Technologies(ISCIT), Sept 2014, pages 400-403, doi:10.1109/ISCIT.2014.7011941

[16] Jadav ChandraDas, Debashis De and Tapatosh Sadu.” A novel low power nano scale reversible decoder using quantum dot cellular automata for nano communication”, Third International Conferrence on devices, circuits and systems, 2016.

[17] Ritjit Maumdar, sandeep saini “ A novel design of reversible 2: 4 decoder”,978-1-4799-6761-2/$31.00©2015 IEEE.

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